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The Design of an Efficient Low-cost FPGA-based Unit for Generation Ultrasound Beamforming

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ABSTRACT

One of the most critical steps in forming an ultrasound image is beamforming, which determines the nature and shape of the sound waves produced. It allows for generating either sound waves focused on a specific depth in the area to be explored (focused beam) or plane waves. The control of the piezoelectric elements forming the probe causes the difference between these modes. In this paper, we focus on generating the commands for the beamforming transmission for both focused and plane wave techniques. The produced signals of the command were applied to the transducers to achieve the desired sound beam. Eventually, we design and implement the algorithm using a low-cost AlTera DE10-lite development board. The results show that despite not optimizing the hardware, the board was able to generate the necessary signals efficiently with less than 4% as logic elements requirement and used memory of 0% in the most complex and demanding scenario. Given the speed of access they present, we replace the use of memory with registers.

Keywords: Focused beamforming, low-cost FPGA platform, plane waves, ultrasound

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Ultrasound is one of the most used medical

INTRODUCTION

imaging modalities thanks to its multiple benefits, including ease of use, patient and doctor safety, and, most importantly, portability (Maeda et al., 2012). Thanks to its underlying technology and principal component, the probe -often small in size-

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makes it easy to carry and move; ultrasound is considered one of the highly coveted tools in medical imaging.

Nevertheless, the major disadvantage of this medical imaging technique lies in the image quality compared to MRI or even X-ray. The ultrasound image suffers from artifacts that decrease its quality in resolution and contrast; consequently, several works have been done to improve the quality of the image. These works have targeted one or more specific parts of the ultrasound image production process.

Beamforming is among the most scrutinized areas for potential enhancements of ultrasound image resolution. Many works have been published in this area showing the beamforming impact on image quality. Demi (2018) presents a work as a guide for Ultrasound Beamforming where the quality of each technique is discussed. Agarwal et al. (2016) propose an architecture of a real-time delay calculator for digital-focused beamforming in an ultrasound imaging system using a curved probe. In Tanter and Fink (2014), the authors have presented plane waves (PW) as an ultrafast imaging technique that directly affects signal processing speed. Tang et al. (2021) admit the ability of PW to improve frame rate; they accordingly suggest a reconstruction method via attention mechanism and Unet-based GAN (AUGAN) to improve the resolution quality. Liebgott et al. (2016) have launched a challenge that presented a cornerstone for all the work that has followed and prompted us to develop a suitable interface command to generate PW.

FPGA provides a very appealing option that balances high flexibility, design cycle, affordability, and performance (Seng et al., 2021). Nowadays, (FPGA) can be realized in millions of logic gates thanks to the new advances in IC design technology (Babu & Parthasarathy, 2021). The FPGA has configurable logic blocks (CLBs) that contain flip-flops and look-up tables (LUTs), allowing the platform to perform various logic functions.

Several works have been carried out to optimize the implementation of different architectures to reduce the resources used or refine the results obtained. Assef et al. (2012) present a digital beamformer system transmission for generating simultaneous arbitrary waveforms to command just 8 channels. In this respect, we have achieved an implementation of 8 times more efficient and 15 times cheaper. Almekkawy et al. (2014) used a mid-range FPGA chip Altera Arria V FPGA to implement a full dynamic beamformer by using the implementation of the delay summation through a bulk (coarse) delay and fractional (fine) delay in the reception process.

Agarwal et al. (2021) proposed implementing a compact architecture of the reception beamformer using a hardware-efficient dynamic delay calculator. They use an adaptive apodization system architecture based on an IEEE single-precision arithmetic and a focusing mechanism to produce high-quality B-mode images, and the presented architecture uses only 60% of the Xilinx Virtex5 XC5VLX330 FPGA hardware resources. Risser et al. (2021) used a very powerful device: the 1024-channel DiPhAS compared to the FPGAs mentioned above regarding channel handling, with the main advantage of controlling all elements simultaneously without multiplexers. The DiPhAS consists of four individual 256-channel systems. Kidav et al. (2022) propose a hardware solution integrating the analog front-end using mid-range FPGA Xilinx® Kintex-7 to command 128 channels. Boni et al. (2018) present an open-source platform where all the different parts responsible for producing the sound waves, as well as the reception of the echoes and their treatment until the formation of the ultrasound image, were well described. This work deeply dissects a commercial ultrasound scanner that clearly shows the separation between its parts, motivating us to produce this paper.

In this article, we propose the implementation of an efficient, low-cost FPGA to generate commands, allowing the production of two beamforming techniques, focused beam and plane wave (PW). The implementation is done on a low-cost FPGA DE10-lite Development Board. In addition, the MAX 10 FPGA on the DE10 lite board used in this work has hardcore memory blocks called SDRAM to address the rising demand for memory to execute complex mathematical operations and sequential tasks. Also, it provides a 32-bit processor called NIOS II.

Ultrasound Hardware

The ultrasonic medical image creation chain encompasses the probe, control system, transmission process, reception process, switch, and monitor, which are the essential components of an ultrasonic image system, as depicted in the block diagram (Figure 1). Transducers, piezoelectric components that emit wave sound and translate received echoes into a signal, make up the probe, a crucial component of an ultrasonic system; it presents a central part of the probe (Figure 2).



Figure 1. Block diagram of the ultrasound imaging system

The probe consists of small adjacent elements called transducers, as shown in Figure 2 (Powles et al., 2018); the transducer activities will be split into two stages, the first of which is known as the excitation stage and lasts 1% of the total duration (Hoskins et al., 2010). During this phase, the transducer only creates soundwave pulses. The second stage is the hearing phase, when the transducer gets echoes; this phase is critical for picture quality.





Figure 2. The probe

the way the transducers are controlled. Each specific control of the transducers gives a sound beam of a specific shape (Figure 3), from which comes the necessity to dedicate this work to generating the different controls that could be applied to the probe elements. This mission is entrusted to an FPGA board able to control simultaneously a consequent number of elements.

Pulser is a driver that excites transducers and controls frequency and voltage amplitude, the two components of an electric pulse (Tan et al., 2020). It is a dedicated circuit to generate high-voltage short-time pulses needed to generate ultrasound, particularly in high-power and high-frequency ultrasonic waves (over a frequency of 1 MHz). Our work focused on



Figure 3. Phased array beam focusing

developing a pulser command system that controls the time when the pulser triggers the transducer.

The reception process by Rossi and Boni (2021) represents the process of data acquisition from the transducers; at its input, we find in generally DAC an analog-to-digital converter that samples the signals of the echoes acquired by the elements of the probe, then it converts these samples into digital information, considering the number of transducers to manage simultaneously, it is consistent, the management of different DAC is relegated to an FPGA board often more powerful than that one used in the pulser command generation. As mentioned earlier, the acquired data is processed using a DSP, a processor dedicated to signal processing, which the FPGA also manages.

The system controller's role is to manage the tasks between the transmission and reception parts, the storage of the data on memory, and the display of the ultrasound information in B-mode, and it prints the image if required. The System controller is generally a sequential processing unit, a microprocessor, or a microcontroller whose program is written in a memory, often of the flash type.

The Switcher module is used to multiplex the transmitter/receiver and protects the receiver against high voltage pulses generated by the pulser.

METHODS

Ultrasound Beams

After we have discussed the primary component that formed the ultrasound system, in this part, we write about the probe command method, which influences the lateral resolution. Thus, the lateral resolution is high when the width of the ultrasound beam is narrow (Dangoury et al., 2020). The shape of the ultrasound beam is crucial for detecting more details at all the image depths. However, unfortunately, we cannot keep control of the shape of the beam because it diverges rapidly after being transmitted.

There are several techniques to control the beam shape; they differ in the performance that each presents.

Focusing

This method allows the probe to focus the beam on a single point at a given scan line, resulting in a very narrow beam with concentrated power throughout this point (Figure 3), which is likely to increase lateral resolution significantly in the specific area but at the expense of frame rate due to its computational demands.

To get a focused signal at a certain point, every single pulser transmission from the active aperture must reach that point simultaneously, which we might accomplish by adjusting the excitation delay between the various elements that make up the aperture



Figure 4. Creating a transmission focus for a phased array: (a) focusing on a left targeted point; and (b) focusing on a right targeted point

(Figure 4). The farthest elements from the scan line are fired first, followed by the center-most elements, the final element to fire. The delay between the applied pulses defines the depth of the focal point; a deeper focal point is achieved by closing the delay difference between the elements, and a closer focal point to the probe is reached by increasing the delay difference between elements.

The practical calculation of the necessary delay for each element will be calculated according to the procedure presented in Figure 5.

Assuming the speed of sound is constant through the explored region, to know the



Figure 5. Array geometry for transmission of a focused beam

Note. N: is the number of elements of the array; *k*: is the index of the array element; *d*: is the pitch or centerto-center distance between two consecutive elements $[m]; d_{f}$ is the distance to the center of the array [m];*d_k*: is the distance to the k element of the array [m]; x_k : is the distance from the k element's center to the center of the array [m].

value of the applied delay for each probe's element, we need to determine the distance between a specific element and the focal point (Figure 5) using Equation 1.

$$d_k = \sqrt{x_k^2 + d_f^2 + 2x_k d_f \sin \alpha} \tag{1}$$

Where x_k is the distance from the center of the array to the k element concerned with excitation, we have Equation 2:

$$x_k = \left(\frac{N-1}{2} - k\right)d\tag{2}$$

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$$d_k = \sqrt{(d_f \cos \alpha)^2 + (d_f \sin \alpha + (\frac{N-1}{2} - k)d)^2}$$
(3)

From all of the above, we express delay as in Equation 4:

$$t_k = t_o - \frac{d_k}{c} \tag{4}$$

where c is the sound speed, and t_o is the time required for a sound wave to reach the focal point from the first excited element.

The Plane Wave

Plane Wave is a technique yielding ultrafast imaging; it uses one generated ultrasound beam through the entire medium by firing all the probe's elements simultaneously, using parallel processing.

Lack of focusing the beam on the transmission phase, the received echoes provide weak information about the heterogeneities of the medium, which leads to forming a b-mode image with low resolution. Coherent Plane-Wave Compounding (CPWC) Imaging is proposed at the expense of temporal resolution to enhance image quality. CPWC consists of coherently adding echoes from the same scatter from different angles (Rodriguez-Molares et al., 2015).

Coherent Plane-Wave Compounding Imaging is a multi-image approach that involves capturing shots of an object from several angles. The idea is to transmit ultrasound waves at different angles through the medium (Figure 6) and combine all collected echoes to generate one image with fewer speckles and better contrast (Couture et al., 2012).

By using plane waves, the received signal is altered as a result of the presence of several excitation angles. When the waves are perpendicular to the edge of the organ, they



Figure 6. PW imaging, all transducer elements are fired with different delays: (a) negative excitation angle; and (b) positive excitation angles

become harder, and the ultrasound image quality changes better, resulting in good reflection; however, when they are parallel to the edge, their image becomes hazy due to reduced reflection. Taking multiple images from various angles solves the problem by offering a clear view of the orange edge, reducing the frame rate significantly (Montaldo et al., 2009).

In order to transmit a plane wave at an angle α , (Figure 7), it is necessary to diphase the excitation signals applied to the different elements, which corresponds to applying a delay τ_{TX} that is calculated according to the following Equation 5:

$$\tau_{TX} = \frac{z \times \cos \alpha + x_k \times \sin \alpha}{c} \tag{5}$$



Figure 7. Geometrical model for delay calculation of plane-wave transmission in a linear probe

The time τ_{RX} required to receive reflected echoes from a point in the explored medium with the following coordinate (x, z) is expressed as shown in Equation 6:

$$\tau_{RX} = \frac{z \times \cos \alpha + x_k \times \sin \alpha}{c} \tag{6}$$

with c is the sound velocity in the explored medium, x_k the k'th element's position, as illustrated in Figure 7. As a result, the total time τ_{Total} it takes a plane wave with emission angle α to travel through the explored medium to target with coordinates (x, z) and rebound to the transducer element k, as shown in Figure 7, is expressed as Equation 7:

$$\tau_{Total} = \tau_{TX} + \tau_{RX} \tag{7}$$

FPGA Implementation

The command program is implemented in the platform DE10-lite Development Board from the Altera family (Figure 8). The platform has on MAX 10 10M50DAF484C7G FPGA chip with the capacity of 50K programmable logic elements (combinational logic functions (CLFs)) and logic registers (LRs)). The board runs at the speed of a 50 MHz main clock. It can be increased a few more times with the four PLLs -phase lock loop-embedded on the FPGA chip. The broad also includes dual ADCs; each ADC supports 1 dedicated analog input and 8 dual function pins. The broad provides 36 GPIO and 16 others GPIO, which are fitted for Arduino uses; if there is a need for any additional pins,

the ones allocated for switches, buttons, and LEDs could be used without any problem because 10M50DAF484C7G have 380 GPIO. The algorithm is written in VHDL hardware description language (HDL) and Cpp on eclipse using Quartus Prime 16.1 Lite Edition development platform.

This work is designed to control probes as The P4-2v, a 64-element phased array transducer from Verasonics, which can be used for Cardiac, Paediatrics, and Abdominal applications. Table 1 presents the probe parameters; it allows us to produce a scanning region from reaching 60 mm in depth with an aperture of 60° ($\alpha_{max} = \pm 30^{\circ}$).

RESULTS AND DISCUSSION

Plan Wave Command

For the calculation of delay applied to the individual elements to generate a plane wave with the expected angle, we assume that the probe is located at the point z = 0 (Figure



Figure 8. DE10-lite development board

Table 1
The probe parameters

Parameter	Value	
Number of elements	64	
Pitch	0.30 mm	
Element width	0.27 mm	
Aperture width	19.2 mm	
Elevation focus	50-70 (mm)	
Transmit frequency	1.0 MHz-5.2 MHz	

7), which will significantly simplify Equation 5. Thus, to transmit, in this case, the waves with different angles, the delay applied must be adjusted according to the following new Equation 8:

$$\tau_k = \begin{cases} x_k \sin(\alpha)/c, & \text{for } \alpha < 0\\ (x_k - N) \sin(-\alpha)/c, & \text{for } \alpha > 0 \end{cases}$$
(8)

Where: τ_k is the time delay for the element *k*; x_k is the lateral coordinate of k, the element.; *N*: is the number of elements of the array; α : is the transmission angle; and *c*: represents the speed of sound.

Due to the well-known complexity of the calculation of trigonometric functions and the possible resources that this requires, we have opted for a look-up table that grouped the fraction of sine divided by the velocity, which represent a constant for the same plane wave throughout the all-probe's elements, that was later used in the calculation of the appropriate delays. The total angle of sweep is of the order of 32°; considering the center of the probe as a reference, this results in two sections: the one on the left has a sweep

angle from -16° to 0, and the one on the right 0 to +16°, having chosen 75 Waves plane this gives a progression of 0.426°, taking into account all of these parameters we need to store 38 different values for $\alpha > 0$, we assign them the plus sign and the opposite for alpha $\alpha < 0$, in sum the constant part of the expression to store using Equation 9:

$$\sin(\alpha)/c$$
 (9)

After computing the appropriate delays to be applied to the different elements of the probe, we subsequently have to convert each delay found to a multiple of the minimum time unit that the clock of our board can generate, in our case, is 20 ns, the value obtained will represent the counting base of a 20 bit counter or a down-counter, for each new wave plane the counter is loaded with the appropriate value when it reaches the value the control pulse is triggered (Equation 10).

$$\operatorname{counter}_{k} = \frac{\operatorname{delay}_{k}}{20} \tag{10}$$

The counters do not start counting until they are all loaded; the same clock signal controls them (Figure 9).



Figure 9. Block diagram of the hardwire implementation for plane wave command

The simulation of the command pulses generated by our board was performed under ModelSim, illustrated in Figure 10. Tables 2 and 3 show samples of the results obtained from the application of Equations 8 to 10; the signals applied to the elements

Table 2

The following table shows a sample of the angles produced for the PW and the resulting constant

The angle α	sin(a)	sin(a)/c	
0	0	0	
0,2158	0,003766412	2,44572E-06	
16	0,275637356	0,000178985	

are shown in Figures 10 to 12. However, given the inability to simultaneously display a single image containing all 64 controlled elements, we will show only samples of what the screenshot can show.

According to the result obtained from the simulation (Figures 10, 11 and 12), we can see that our FPGA has been able to create the necessary delays to generate the PW of the desired angle, for example, according to Table 3, to be able to generate

Table 3 The following table gives the necessary delay and the value of the counter that allows it to have a PW of 10°

Element number	${ au}_k$	counter _k	
63	0	0	
62	0,000178985	8949,2648	
61	0,000357971	17898,5296	
60	0,000536956	26847,7944	
3	0,010739118	536955,888	
2	0,010918103	545905,153	
1	0,011097088	554854,418	
0	0,011276074	563803,682	



Figure 10. Shows the first 25 elements controlled to generate a PW at 0° ; all elements will fire once, and no delay is required



Figure 11. shows the first 25 elements controlled to generate a PW at -16°

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Figure 12. Shows the first 25 elements controlled to generate a PW at +16°

a PW of 16° we must apply a delay of 0,011276074 s (11276074 ns) to the third element, to accomplish this, the counter must be loaded with the value 26847, we will only take the integer part, nevertheless, the value produced by our card corresponds to 11276074 (Figure 12) with an error of 4 ns and 2 ns error for the next elements.

Focused Command

In this second part, we are interested in the production of focused beams; this type of beamforming requires another command different from that used previously in the case of PW. In this step, we will concretize what we have already introduced; the calculation of different delays applied to the transducers will be carried out according to the algorithm [Figure 13 (b)], the result obtained will be recorded in a look-up table, after that the outputs will be triggered as indicated in according to the algorithm [Figure 13 (a)].

For the first implementation relating to the PW, in accordance with Table 4, filled by values taken from the compilation report, the consumed circuit is of the average of 4% max; however, at this stage, the hard is not optimized; we have not used specific IP or PLL for PW for example, which suggests that all the performances of the card are not or less exploited. Therefore, we conclude that this inexpensive card could ensure applications of control of probes larger than that of 64 elements proposed in this work, for example, the control of a linear probe that goes up to 192 elements. Our work is compared to previous work cited in the literature in Table 5.

CONCLUSION

The primary goal of this paper was to investigate the performance of the DE10-lite Development Board for controlling and commanding probe applications. Although this

Start triggering outputs elements triggered $\alpha = \alpha + 1$ k = 0 $d_{max} = d_0$ Set depth ---> d_f Initialization $d_{max} = d_{63}$ 9 START $\alpha > +16^{\circ}$ k = k + 0K > 63 $\alpha \leq +0^{\circ}$ K > 63 k = 0¢. $\mathfrak{T}_k \equiv$ $\left[x_k^2 + d_f^2 + 2x_k d_f \sin \alpha\right]$ -k d k = k + 1 $\left(\frac{N-1}{2}\right)$ $x_k = ($ Ш ď 1,645/49,760 (3%) 0/1,677,312 (0%) 185/360 (51%) The resources used by the board for the two proposed implementations $\mathsf{Delay}_{\tau_{63}}$ after 20 ns Focusing 0/4 (25%) 0/2 (50%) $X_{63} = 0$ $X_{63} = 1$ 1219 Start triggering outputs 378/49,760 (< 1%) Start triggering outputs 185/360 (51%) 295 ΡW (a) after 20 ns 0 Delay_{τ_1} 0 0 $X_1 = 1$ $X_1 = 0$ Element number $\mathsf{Delay}_{ au_0}$ Logic elements after 20 ns $X_0 = 1$ $X_0 = 0$ Memory bits ADC blocks Registers PLLs Table 4 Pins

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Figure 13. (a) and (b) are the organigram implemented in software application

	Our project	(Assef et al., 2012)	(Almekkawy et al., 2014)	(Agarwal et al., 2021)	(Kidav et al., 2022)
Device	Altera MAX 10 FPGA	Altera Cyclone III FPGA	Altera Arria V FPGA	Xilinx Virtex 5 FPGA	Xilinx Kintex-7 FPGA
Channel	64	8	64	64	128
Logic cells	50K	-	64,986	-	162,240
Frequency	50 MHz	20 MHz	12 MHz	40 MHz	65 MHz
Phase adjustment:	32°	$0^{\circ} \pm 360$	-	-	-
The angular resolution	0.426°	7.5° per step	-	-	-
Price	82 \$	1512 \$	$+800 \$	+109\$	+450\$

Table 5Comparison to previous work in the literature

work did not fully utilize all the board's capabilities and features, it demonstrated that low-cost FPGAs are adequate for controlling the excitation of transducers. The excitation produced by the board was consistent with the study's analysis and adhered to all the instructions in the study's theory.

The test results showed that the board could effectively produce the desired signals using less than 4% of the required logic components and 0% of the total memory usage in the most demanding scenario, the focused beam (Figure 14). The optimization of the algorithm's implementation using only logical registers allowed for fast access and memory savings for other tasks. It suggests reserving a more powerful board solely for acquisition and signal processing.



Figure 14. Shows the first 25 elements controlled to generate a focused beam at the point with a depth of 30 mm and -16°

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Future work will investigate modifying the PLLs provided by the FPGA board to control larger probes while increasing the frequency. Overall, this work has demonstrated that the DE10-lite Development Board is a suitable and cost-effective option for controlling and commanding probe applications. The results presented in this paper provide valuable insights for researchers and engineers working on similar projects.

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